(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
24 July 2003 (24.07.2003)

PCT

(10) International Publication Number
WO 03/061109 A1

(51) International Patent Classification[7]: H03B 5/18, H03K 3/03

(21) International Application Number: PCT/US03/00932

(22) International Filing Date: 13 January 2003 (13.01.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/347,415 11 January 2002 (11.01.2002) US

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, SE, SI,

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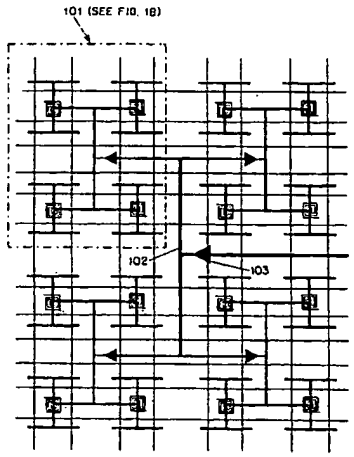
(54) Title: RESONANT CLOCK DISTRIBUTION FOR VERY LARGE SCALE INTEGRATED CIRCUITS

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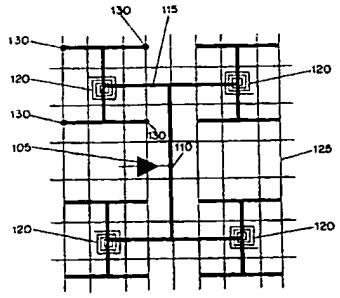


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(57) Abstract: A circuit for distributing a clock signal in an integrated circuit includes a capacitive clock distribution circuit (102) having at least conductor (115) therein. At least one inductor is formed in a metal layer of the integrated circuit and is coupled to the clock distribution circuit. The inductor, generally in the form of a number of spiral inductors (120) distributed throughout the integrated circuit, provides an inductance value selected to resonate with the capacitive clock distribution circuit at resonance, power dissipation is reduced while skew and jitter performance can be improved.

WO 03/061109 A1

SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

# RESONANT CLOCK DISTRIBUTION FOR VERY LARGE SCALE INTEGRATED CIRCUITS

## FIELD OF THE INVENTION

The present invention relates generally to clock distribution in integrated circuits and more particularly relates to methods of distributing a high frequency clock with improved power efficiency and skew and jitter performance.

## BACKGROUND OF THE INVENTION

Clocking large digital chips with a single high-frequency global clock is becoming an increasingly difficult task. As circuit size and clock frequency continue to increase, skew and jitter as well as power consumption are becoming increasingly important design considerations.

While jitter and skew have traditionally been the dominant concerns in clock circuit design, power consumption may soon gain primacy. With each new generation of integrated circuit, clock capacitance and frequency are increasing resulting in significant increases in dynamic power dissipation. Considering that a 72-W 600-MHz Alpha processor dissipates more than half of its power in the clock circuit, this is clearly an area ripe for design optimization.

To date, most of the work in clock distribution has been focused on addressing the issues of skew and jitter. There are two general approaches to clock wiring, trees and grids. Tunable trees consume less wiring and, therefore, represent less capacitance, lower wiring track usage, lower power, and lower latency. Trees must, however, be carefully tuned and this tuning is a very strong function of load. Thus, there is substantial interplay between the clock distribution circuit and the underlying circuit being driven by the clock circuit. Grids, in contrast, can present large capacitance and require significant use of wiring resources, but provide relative load independence by connecting nearby points directly to the grid. This latter property has proven irresistible and most recent global clock distributions in high-end microprocessors utilize some sort of global clock grid. Early grid distributions were driven by a single effective global clock driver positioned at the center of the chip.

Most modern clock distribution circuits use a balanced H-tree to build up and distribute the gain required to drive the grid. The grid drive points are

distributed across the entire chip, rather than being concentrated at a single point; this means that the grid can be less dense than a grid that is driven in a less distributed fashion, resulting in less capacitance and less consumption of wiring resources. The shunting properties of the grid help to cancel out skew and jitter from imperfections in the tree distribution, as well as balance out uneven clock loads.

To prevent skew and jitter from accumulating with increased distance from the clock source, there have been several approaches for using multiple on-chip clock sources. One approach is to create a distributed phase-locked loop (PLL) in which there is a single phase-frequency detector, charge pump, and low-pass filter, but multiple voltage-controlled oscillators (VCOs). These oscillators are distributed across the chip to drive a single clock grid. The grid acts to help cancel out across-chip mismatches between the VCOs and limit skew and cycle-to-cycle jitter. The main problem with this approach is the need to distribute a "global" analog voltage across the chip (the VCO control voltage), which can be very susceptible to noise.

An alternative to this approach is to have multiple PLLs across the chip, each driving the clock to only a small section or tile of the integrated circuit. Clock latency from the oscillator is reduced because the clock distribution is local and the clock loads for each PLL is smaller. In such a design, each PLL must average the phases of its neighbors to determine lock and nonlinearities must be introduced into the phase detectors to avoid mode-locked conditions. Any mismatch between the phase detectors adds uncompensated skew to the distribution.

To control clock power, the most common technique employed is that of clock gating, in which logic is introduced into the local clock distribution to ``shut off" the clocking of sections of the design when they are not in use. These techniques generally favor relegating more of the clock load to ``local" clocking where it can be gated and have been widely employed in low-performance designs in which power is of prominent concern (e. g. digital signal processors for mobile, battery-powered applications). Until recently, clock gating has not been favored as a technique for high-performance design because of the skew and jitter potentially introduced by the clock gating logic and because of delta-I noise concerns (i. e., transients introduced in the power supply distribution when large amounts of switching clock capacitance are turned on and off.) As clock power exceeds 80 W, clock gating is beginning to be employed even in these high-performance chips.

The natural limit of clock gating is to approach more asynchronous design techniques, in which blocks are activated only in the presence of data. Globally-asynchronous, locally synchronous (GALS) design preserves the paradigm of synchronous design locally. Asynchronous design techniques, however, are more difficult to design, costlier to implement, more challenging to test, and more difficult to verify and debug. There is clearly a significant desire to continue to use and improve upon globally synchronous designs.

The virtues of LC-type oscillators for achieving lower-power and better phase stability (than oscillators based on delay elements) have been long recognized. The adiabatic logic community has already considered the importance of resonant clock generation since the clocks are used to power the circuits and such resonance is fundamental to the energy recovery. These generators generally produce sinusoidal or near sinusoidal clock waveforms. To combine the clock generation and distribution, distributed LC oscillators in the form of transmission line systems have been considered. These also bear resemblance to distributed oscillators. In salphasic clock distribution, a standing (sinusoidal) wave is established in an unterminated transmission line. As a result, each receiver along the line receives a sine wave of identical phase (but different amplitude). Unfortunately, on-chip transmission lines tend to be very lossy and exhibit low bandwidths for long wire lengths. This produces significant phase error due to the mismatch in amplitude between forward and reverse propagating waves.

Another approach that has been proposed uses a set of coupled transmission line rings as LC tank circuits, pumped by a set of cross-coupled inverters to distribute clock signals. The propagation time around the rings determines the oscillation frequency and different points around the ring have different phases. This approach, however, also has many significant difficulties. Rings must be precisely "tuned" even with potentially varying (lumped) load capacitance producing discontinuities in the transmission line. Fundamentally, the distribution and the resonance determining the clock frequency are fundamentally linked, in which the former may depend on geometry or other constraints inconsistent with the desired resonance frequency.

Another approach to synchronized clock distribution in an integrated circuit is disclosed in United States Patent 6,057,724 to Wann. The Wann patent

discloses a clock distribution circuit which includes a parallel plate microstrip resonator formed in the integrated circuit which operates as a resonant cavity to generate a clock signal.

Despite the various efforts to provide clock distribution circuits for very large scale integrated circuits, there remains a need for a clock distribution circuit which offers lower power consumption without sacrificing, and preferably improving, skew and jitter performance.

## SUMMARY OF THE INVENTION

It is an object of the present invention to provide an integrated circuit clock distribution topology which enables efficient distribution of high speed clock signals in large and very large scale integrated circuits.

It is a further object of the present invention to provide a clock distribution circuit which consumes less power than a conventional clock distribution circuit operating at the same clock speed.

It is a further object of the present invention to provide a clock distribution circuit which consumes less power than a conventional clock distribution circuit operating at the same clock speed while maintaining or improving skew and jitter performance.

It is another object of the present invention to provide a clock distribution circuit in which the clock distribution circuit presents a resonant circuit at the operating frequency of the clock.

In accordance with the present invention, a circuit for distributing a clock signal in an integrated circuit is provided which includes a capacitive clock distribution circuit having at least one conductor therein and at least one inductor formed in a metal layer of the integrated circuit. The inductor(s) is coupled to the conductor and has an inductance value selected to resonate with the capacitive clock distribution circuit.

Preferably, inductor(s) takes the form of a number of inductors, such as spiral inductors, distributed throughout the integrated circuit.

The clock distribution circuit can include a clock grid circuit which is coupled to one or more H-tree driving circuits. In larger integrated circuits, a hierarchical architecture can be employed wherein the integrated circuit is partitioned

into a plurality of sectors with each sector being driven by an H-tree and the sector-based H-trees being driven by at least one further H-tree distribution circuit.

In another embodiment in accordance with the present invention, a clock distribution circuit includes a clock driver circuit which is coupled to a clock distribution circuit. The clock distribution circuit presents a clock circuit capacitance to the clock driver circuit. A number of inductors are coupled to the clock grid circuit. The inductors are spatially distributed about the clock grid circuit and present a total inductance value which is substantially resonant with the clock circuit capacitance at the operating frequency of the clock driver circuit.

The clock distribution circuit can include a clock grid which is coupled to one or more tree distribution circuits. The clock driver circuit can include a master clock which is provided to one or more buffer amplifiers throughout the integrated circuit. Alternatively, the clock driver circuit can be formed with a number of synchronized phase lock loop circuits coupled to the clock grid circuit.

To optimize the Q of the resonant clock circuit, the capacitance of the clock distribution circuit can be tuned by including one or more capacitors which can be selectively switched into or out of the clock distribution circuit to optimize the circuit resonance.

## BRIEF DESCRIPTION OF THE DRAWING

Further objects, features and advantages of the invention will become apparent from the following detailed description taken in conjunction with the accompanying figures showing illustrative embodiments of the invention, in which:

Figure 1A is a pictorial view of a resonant clock distribution circuit in accordance with the present invention;

Figure 1B is a detailed view of one sector of the resonant clock distribution circuit of Figure 1A;

Figure 2 is a perspective view illustrating the fingering and shielding of clock grid wires which maintains a low stray inductance in the clock circuit; and

Figure 3 is a schematic diagram illustrating a simplified lumped element equivalent circuit of the resonant clock distribution circuit of the present invention.

Throughout the figures, the same reference numerals and characters, unless otherwise stated, are used to denote like features, elements, components or portions of the illustrated embodiments. Moreover, while the subject invention will now be described in detail with reference to the figures, it is done so in connection with the illustrative embodiments. It is intended that changes and modifications can be made to the described embodiments without departing from the true scope and spirit of the subject invention as defined by the appended claims.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention provides a circuit topology and design method for distributing a clock signal within an integrated circuit. The present invention provides a clock distribution circuit which is substantially resonant at the clocking frequency such that power efficiency is improved and skew and jitter is minimized.

Figure 1A is pictorial diagrams illustrating a top planar view of an embodiment of the present resonant clock distribution circuit as viewed through a number of metalization layers of an integrated circuit. The circuit of Figure 1B illustrates a single sector 101 of the circuit of Figure 1A. The circuit of Figure 1B may represent a sector having an area of about 2,500 μM x 2,500 μM. A typical microprocessor clock distribution may include several dozen of such clock distribution sectors, which are coupled together to provide a global clock distribution circuit. The circuit of Figure 1A illustrates the circuit of Figure 1B implemented in four adjacent sectors of an integrated circuit with the four sectors 101 being driven by a further clock distribution circuit, such as an H-tree 102, to deliver the clock signal from a master clock 103 to the individual sector driver circuits. It will be appreciated that while Figure 1A illustrates an exemplary interconnection of adjacent sectors, this figure still only represents a small portion of an entire integrated circuit. Depending on the size of the integrated circuit, additional hierarchical levels of clock distribution may be provided between the master clock 103 and the individual sectors 101.

Referring to Figure 1B, the circuit for each sector 101 includes a clock driver circuit 105 which is coupled to a conventional H-Tree 115 at central driving point 110. The H-tree 115 is coupled to a clock grid 125 via connection vias 130 in a manner well known in the art. The H-tree 115 and clock grid 125 along with the circuitry coupled to the clock grid 125, present a capacitive load to the clock driver

circuit 105 which is referred to herein as the clock circuit capacitance ($C_{clock}$). The clock driver circuit will generally take the form of a buffer amplifier. However, in certain embodiments, the clock driver circuit 105 may take the form of a local oscillator which is synchronized to a master clock. The present invention employs at least one inductor, and more preferably a number of spiral inductors 120, which are coupled to the clock grid 125 and operate to resonate with the clock circuit capacitance, thereby forming a resonant circuit with the clock grid 125. In the embodiment depicted in Figures 1A and 1B, the spiral inductors 120 have one end coupled directly to the clock grid 125 and the other end to a ground potential via a large decoupling capacitance, not shown,. The use of AC coupling of inductors 120 in this fashion establishes a mid-rail DC voltage about which the clock grid oscillates. This mid-rail DC voltage can be used as a reference voltage in a pseudodifferential switching circuit. The decoupling capacitors can be formed as thin-oxide capacitors which are located in the integrated circuit below each spiral inductor 120 within the active device layer.

The clock tree 115 is typically formed on the top two metal layers (e.g., M6 and M5 layers) of the integrated circuit and the clock grid 125 is formed on the top three metal layers (e.g., M6, M5, M4 layers) of the integrated circuit. The clock grid 125 is formed as a regular mesh using 1.5 μm wide line segments which are fingered 0.5 μm apart. As illustrated in Figure 2, it is preferable for each clock line of the clock tree 115 and clock grid 125 to be split into finger segments 205 and shielded with ground segments 210 on either side and between the clock distribution line segments. The clock tree 115 is formed using 10 μm wide line segments spaced 0.5 μm apart. For the sake of clarity, the grid for power distribution, which is generally formed on the M4, M5 and M6 layers, has been omitted from the diagram in Figure 1.

The spiral inductors 120 are fabricated on the top two metal layers and are formed with a spiral length, spacing and line width to present an inductance value that will substantially resonate with the capacitance presented by the clock tree 115 and clock grid 125 at the desired clock frequency.

The clock grid 125 generally presents a capacitive load in which the stray inductance is low. By way of a mechanical analogy, the capacitive clock grid 125 operating at resonance with the spiral inductors 120 can be viewed as a rigid mass

which is supported by a number of springs and oscillates as a unit. Thus, at resonance, the entire clock grid 125 is oscillating in phase.

In contrast to the methods of clock distribution which utilize a standing wave in the distribution circuit, by virtue of the spiral inductors and low inductance of the grid circuit, the present circuit presents an eigenmode of the grid in which it rigidly oscillates as a contiguous unit at the clock frequency ($f_{clock}$). By taking steps to insure that the grid presents a low inductance, such as by fingering the clock distribution and grid conductors, unwanted resonances generally associated with the distribution circuit are pushed to high frequencies so that they do not interfere with the engineered resonance at $f_{clock}$.

It will be appreciated that in the present clock distribution circuits, the spiral inductors exist in an environment quite different from those that are presented in typical radio frequency (RF) applications in which these components are generally used. Specifically, the inductors 120 embedded in the metal-rich environment of a digital integrated circuit. As such, eddy current losses due to neighboring wires should be considered and minimized. Such eddy current losses will result in Q degradation of the resulting resonant clock circuit and may result in inductive noise in the power-ground distribution or in neighboring signal lines. Because the spiral inductors are generally much larger than the power grid, most of the potential deleterious coupling will be to the underlying power grid. To reduce eddy current formation in the underlying grid, the vias in the grid can be dropped and small cuts can be made in the wires. This technique is generally known to those skilled in the art of RF circuit design as it is analogous to ground plane laminations used for spiral inductors in RF circuits.

Figure 3 is a schematic diagram illustrating a simplified equivalent circuit diagram for the resonant clock distribution circuit for one sector of an integrated circuit, such as shown in Figure 1B. The clock driver 105 is represented as signal source 300 and series resistance $R_{driver}$ 305. The clock capacitance for the sector, including the clock grid 125, clock tree 115 and circuitry coupled thereto, is represented by a series RC circuit of $R_{cap}$ 310 and $C_{clock}$ 315. Spiral inductors 120 are represented by a series RL circuit with inductor L 320 and resistor R 325. The decoupling capacitor, which couples the spiral inductor to ground is represented by capacitor $C_{decap}$ 330.

The decoupling capacitor $C_{decap}$ 330 is chosen to have a value large enough such that the resonance formed with the inductor 320 is much lower in frequency than the desired resonant frequency of the clock grid and clock tree. Therefore, $C_{decap}$ 330 will generally have a value substantially larger than $C_{clock}$ 315. For example, setting $C_{decap}$ 330 at a value approximately ten times larger than $C_{clock}$ 315 is expected to provide adequate results. When this is achieved, the driving point admittance of the clock distribution circuit is substantially determined by the clock capacitance and inductance of inductors 320. This is expressed as:

$$Y_{driver} = j\omega ( C_{clock} - 1/(L\omega^2))$$

The inductance value of inductor 320 is selected such that the capacitive reactance of $C_{clock}$ is resonated out by the inductive reactance of inductor 320. When the circuit is substantially resonant at the clock frequency, rather than having the clock energy dissipated as heat during each clock cycle, a significant portion of the energy of the clock is converted from electrical to magnetic energy and back. This substantially non-dissipative power conversion process reduces the power consumption of the clock distribution thereby increasing efficiency. The improved efficiency also means that less heat needs to be dissipated by the device which can reduce heat sinking and venting requirements for the resulting integrated circuit.

While in the equivalent circuit of Figure 3 the spiral inductors 120 are represented by a single inductance L 320 it is beneficial to distribute this total inductance using a large number of inductors 120 distributed throughout the grid as illustrated in Figures 1A and 1B. It will be appreciated that the spiral inductors 120 are coupled together as a parallel circuit. Thus, for a 1GHz clock distributed on a clock grid 125 for a sector having a capacitance of 100 pf, approximately 250 pH of inductance is required to form a resonant circuit. This 250 pH inductance can be obtained by use of four (4 ) 1nH spiral inductors distributed throughout the grid, as illustrated in Figure 1B. A 1nH spiral inductor can be formed in an area of about 100 μm square using 3 turns of 5 μm wide line segments. Distributing the inductance throughout the clock grid serves to reduce the peak current density through each inductor and balances the current distribution throughout the clock grid 125.

As with other generally known resonant circuits, the Q factor of the resonance of the clock circuit of the present invention effects the quality of the results. When the Q is higher, the clock driver circuits can be made weaker since there is less

loss that must be overcome at the fundamental clock frequency. This is desirable as a weaker driver consumes less power and presents less skew and jitter. However, use of a weak driver tends to result in a more sinusoidal clock signal. When the Q is poor, the drivers must be larger to overcome the losses of the clock circuit. More power is dissipated in the distribution not only because more energy must be provided at the fundamental to overcome losses, but also due to lossy higher frequency components that are also being driven in the clock network by the drivers. Thus, efficiency is reduced.

Typically, the Q factor which is obtained in the embodiments described herein is on the order of 3-5. Higher Q values may be desirable to further improve power savings and skew and jitter performance. As higher Q values are obtained, the desirability of tuning the circuit becomes more significant. The present clock distribution can be tuned by including one or more MOS capacitors which are selectively coupled to the clock grid or distribution circuit, such as by MOS switches.

Skew and jitter in conventional clock distribution networks comes about because of spatial and temporal variation, respectively, in the clock latency. A significant component to skew and jitter is variation in the latency of the buffering (or gain) stages needed to drive the large capacitive load of the clock network. Across die variability, sometimes referred to as across-chip linewidth variation, or ACLV, is a significant source of skew and power-supply noise, which when coupled through the buffers, is a significant source of jitter. Resonant clock distribution circuits of the present invention can significantly reduce this component of clock latency by reducing the size of clock drivers, which can result in improved skew and jitter performance.

In the embodiment shown in Figures 1A and 1B, a hierarchical H tree distribution scheme is used to distribute a master clock driver signal throughout an integrated circuit to a number of distributed drivers in the individual sectors of an integrated circuit. It will be appreciated that various other clock distribution schemes can be used to drive the resonant clock circuit. For example, multiple phase lock loop circuits can be distributed throughout the clock grid with the PLLs driving the grid and being locked thereto. In this case, one of the PLL circuits is referenced to an external clock and the remaining PLLs synchronize to this master PLL. In this form of clock distribution, mode-locking, wherein the system is stable with non-zero relative

phase difference between the PLLs, needs to be avoided. Should mode locking occur, significant short circuit current would flow.

During normal operating conditions, the circuit is intended to operate at the clock frequency at which the circuit is resonant. However, it is well known in the art that certain operations of an integrated circuit, such as during manufacturing testing or debugging operations, occur at clock frequencies well below the normal clock frequency. It will be appreciated that the present clock distribution circuits do not prevent such reduced frequency operations.

Although the present invention has been described in connection with specific exemplary embodiments, it should be understood that various changes, substitutions and alterations can be made to the disclosed embodiments without departing from the spirit and scope of the invention as set forth in the appended claims.

WHAT IS CLAIMED IS:

1. A circuit for distributing a clock signal in an integrated circuit having a plurality of metal layers therein, comprising:

a capacitive clock distribution circuit having at least conductor therein; and

at least one inductor formed in a metal layer of the integrated circuit, said inductor being coupled to said at least one conductor and having an inductance value selected to resonate with the capacitive clock distribution circuit.

2. The circuit for distributing a clock signal, as defined by claim 1, wherein the at least one conductor in the clock distribution circuit includes a clock grid.

3. The circuit for distributing a clock signal, as defined by claim 2, wherein the at least one conductor in the clock distribution circuit further includes a tree distribution circuit coupled to the clock grid.

4. The circuit for distributing a clock signal, as defined by claim 3, wherein the integrated circuit has a plurality of operating sectors and wherein the at least one conductor further comprises a tree distribution circuit corresponding to each of the sectors of the integrated circuit.

5. The circuit for distributing a clock signal, as defined by claim 1, wherein the at least one inductor includes a plurality of inductors distributed on the clock distribution circuit.

6. The circuit for distributing a clock signal, as defined by claim 5, wherein the plurality of inductors take the form of spiral inductors.

7. The circuit for distributing a clock signal, as defined by claim 6, further comprising a plurality of decoupling capacitors formed in the integrated circuit, the plurality of decoupling capacitors corresponding to the plurality of spiral inductors, wherein the spiral inductors are coupled to a power-ground grid potential in the integrated circuit by a corresponding decoupling capacitor.

8. The circuit for distributing a clock signal, as defined by claim 1, further comprising a decoupling capacitor formed in the integrated circuit, wherein the at least one inductor is coupled to a power-ground grid potential by a coupling capacitor formed in the integrated circuit.

9. A circuit for providing a clock signal in an integrated circuit comprising:

a clock driver circuit, the clock driver circuit providing a clock signal having a clock frequency;

a clock distribution circuit having at least one conductor therein, the clock distribution circuit being coupled to the clock driver circuit; and

a plurality of inductors coupled to the clock distribution circuit, the plurality of inductors being spatially distributed about the clock distribution circuit and presenting a total inductance value which is substantially resonant with the clock distribution circuit at the clock frequency.

10. The circuit for providing a clock signal, as defined by claim 9, wherein the at least one conductor in the clock distribution circuit includes a clock grid.

11. The circuit for providing a clock signal, as defined by claim 10, wherein the at least one conductor in the clock distribution circuit further includes a tree distribution circuit coupled to the clock grid.

12. The circuit for providing a clock signal, as defined by claim 11, wherein the integrated circuit has a plurality of operating sectors and wherein the at least one conductor further comprises a tree distribution circuit corresponding to each of the sectors of the integrated circuit.

13. The circuit for providing a clock signal, as defined by claim 12, wherein the clock driver circuit includes a plurality of buffer amplifiers, wherein each tree distribution circuit corresponding to a sector is coupled to at least one of the plurality of buffer amplifiers.

14. The circuit for providing a clock signal, as defined by claim 13, wherein the clock distribution circuit includes at least a further tree distribution circuit, said further tree distribution circuit being coupled to the buffer amplifiers in a plurality of sectors of the integrated circuit.

15. The circuit for providing a clock signal, as defined by claim 12, wherein the clock driver circuit comprises a plurality of phase lock loop circuits, wherein each tree distribution circuit corresponding to a sector is coupled to at least one of the plurality of phase lock loop circuits.

16. The circuit for providing a clock signal, as defined by claim 9, wherein the plurality of inductors take the form of spiral inductors.

17. The circuit for providing a clock signal, as defined by claim 16, further comprising a plurality of decoupling capacitors formed in the integrated circuit, the plurality of decoupling capacitors corresponding to the plurality of spiral inductors, wherein the spiral inductors are coupled to a power-ground grid potential in the integrated circuit by a corresponding decoupling capacitor.

18. The circuit for providing a clock signal, as defined by claim 17, wherein a voltage potential at the junction of a spiral inductor and corresponding decoupling capacitor is provided as a reference voltage for psuedodifferential switching of the clock signal.

19. The circuit for providing a clock signal, as defined by claim 9, further comprising at least one capacitor switchably coupled to the clock distribution circuit, whereby the total capacitance of the clock distribution circuit can be tuned by switching said at least one capacitor.

20. A method of distributing a clock signal in an integrated circuit having at least one clock distribution conductor therein, comprising:

determining the capacitance of clock distribution conductor and circuitry coupled thereto;

determining the inductance value required to resonate with the capacitance at a clock frequency; and

coupling at least one inductor to said clock distribution conductor to provide said inductance value.

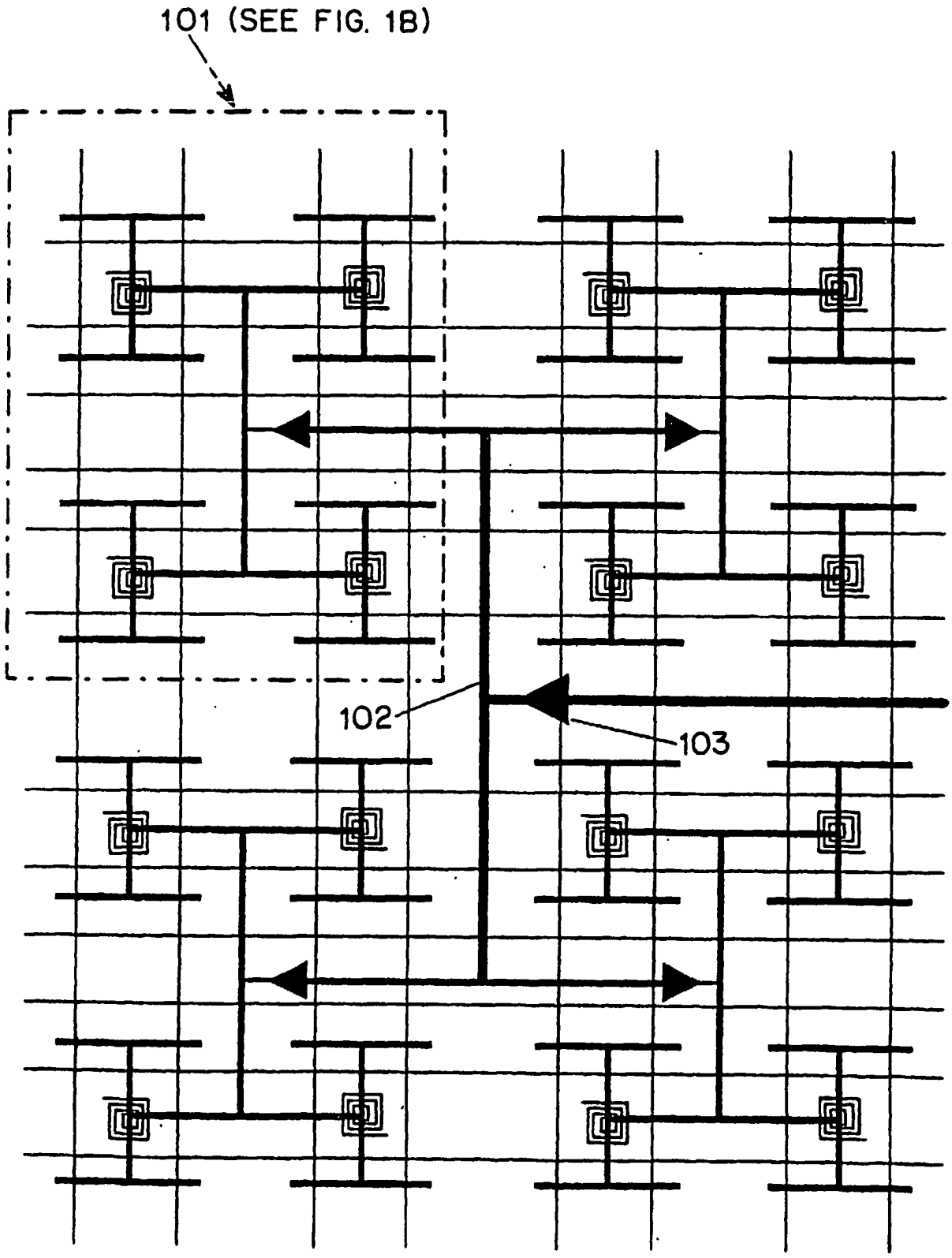



FIG. 1A

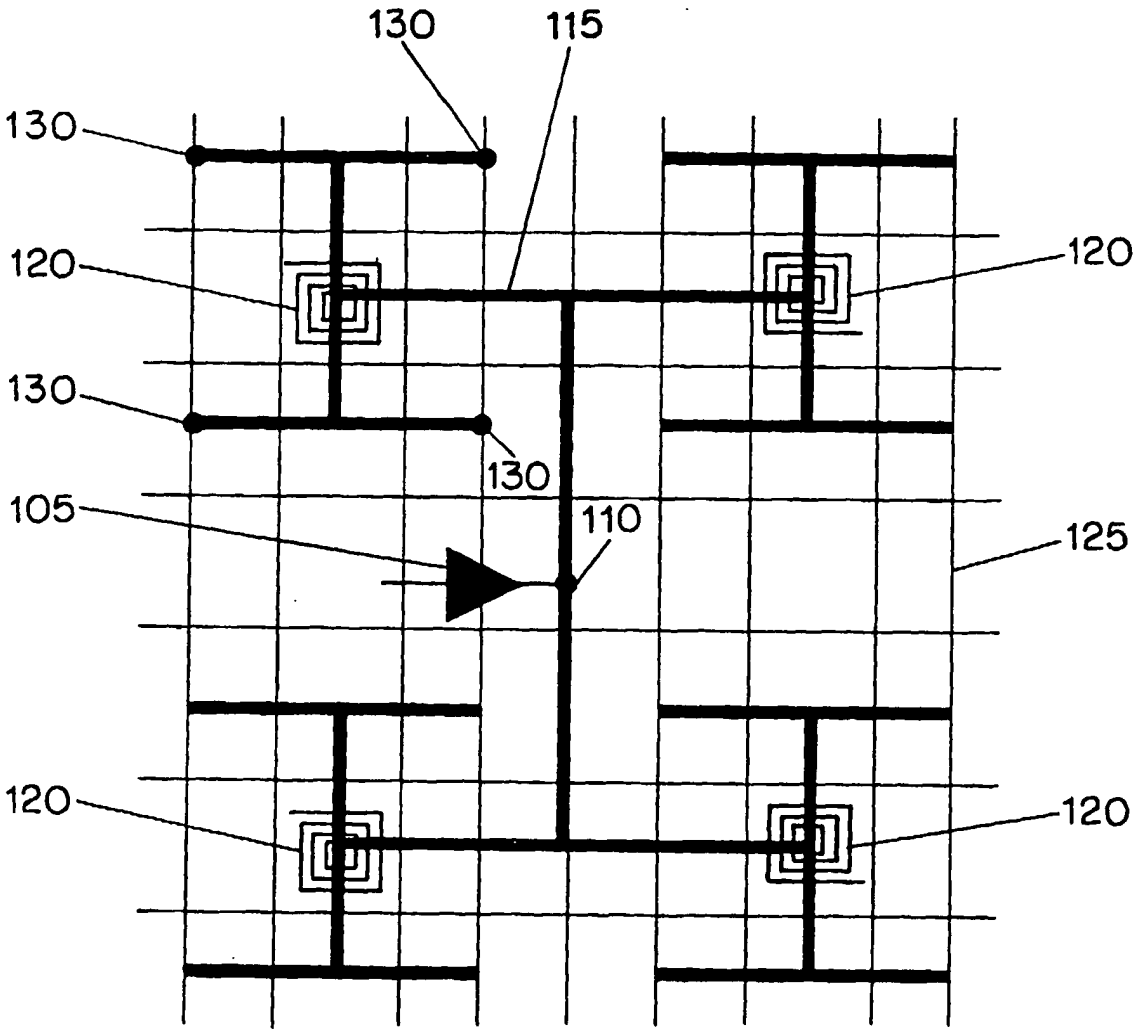
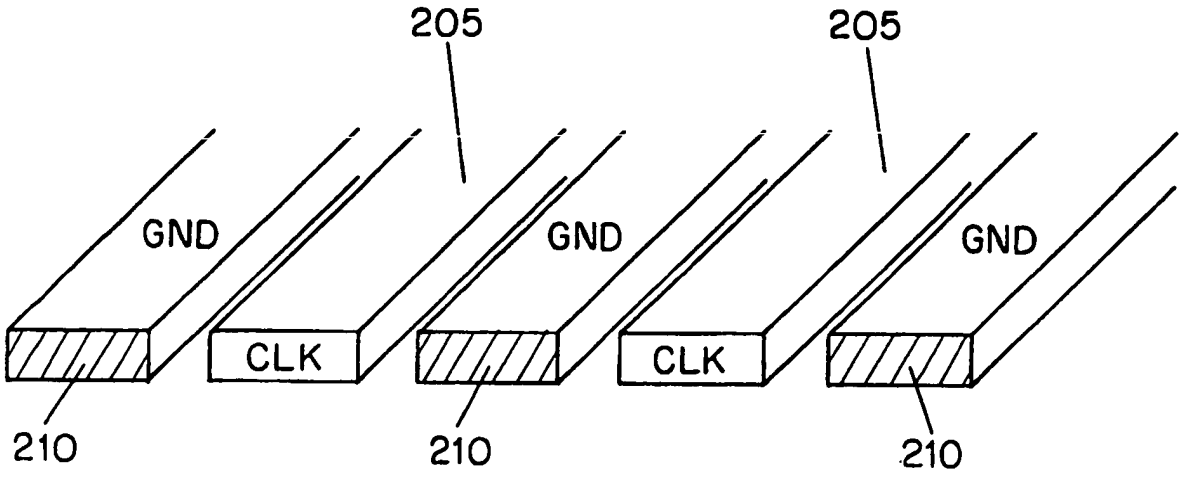



FIG. 1B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205
GND
GND
GND
CLK
CLK
210
210
210

FIG. 2

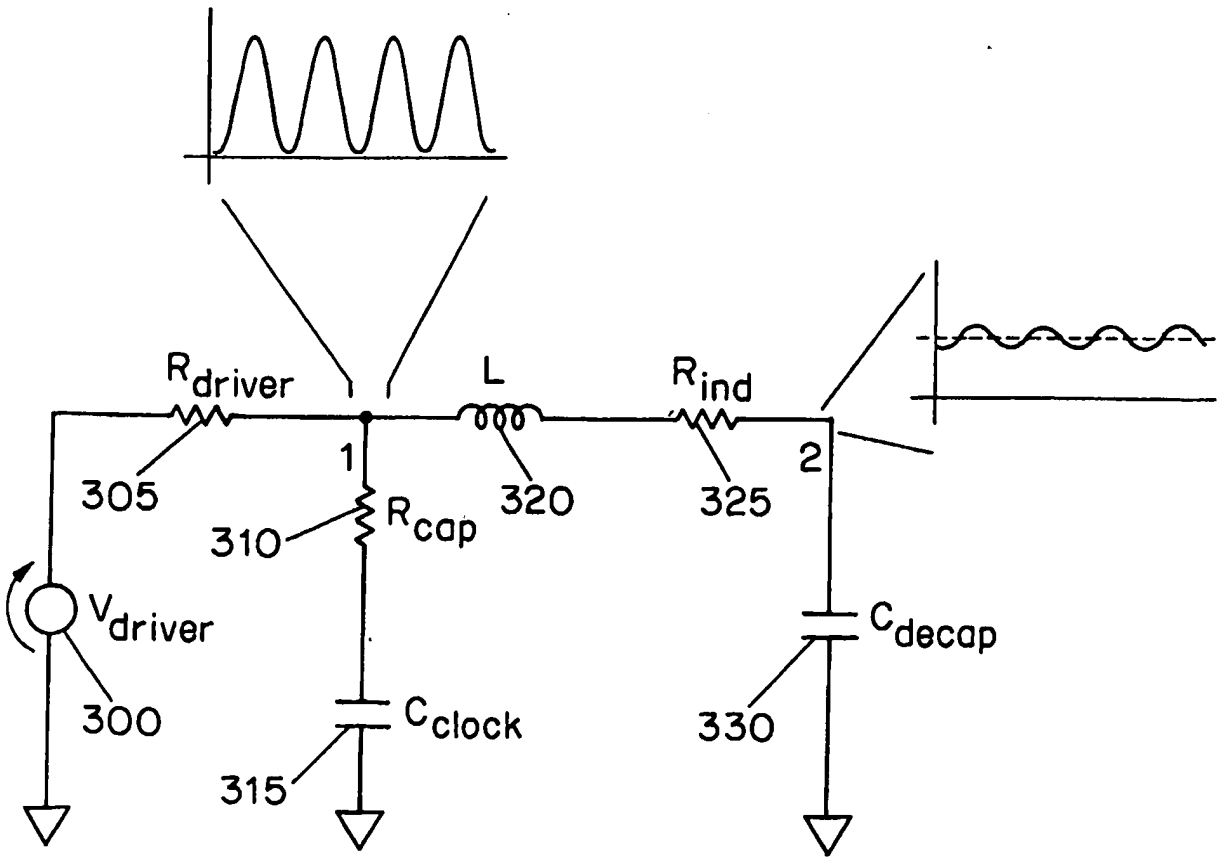
R driver
L
R ind
1
2
305
310
R cap
320
325
V driver
C decap
300
C clock
330
315

FIG. 3

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/00932

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(7) : H03B 5/18; H03K 3/03
US CL : 331/96; 713/ 500, 503

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 331/96; 713/ 500, 503

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| P,X<br>---<br>P,Y | US 2003/0006851 A1 (WOOD) 09 January 2003(09.01.2003), see cols. 5, 7,9 and 12 | 1,9,10,19 and 20<br>---<br>2-8, and 11-18 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 30 April 2003 (30.04.2003) | 04 JUN 2003 |
| Name and mailing address of the ISA/US<br>Mail Stop PCT, Attn: ISA/US<br>Commissioner for Patents<br>P.O. Box 1450<br>Alexandria, Virginia 22313-1450<br>Facsimile No. (703)305-3230 | Authorized officer<br>Arnold M Kinkead<br>Telephone No. 703-308-0956 |

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